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10/824,417	04/15/2004	Jang Hwan Cho	YHK-0111	6471

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KED & ASSOCIATES, LLP
P.O. Box 221200
Chantilly, VA 20153-1200

EXAMINER	
SITTA, GRANT	
ART UNIT	**PAPER NUMBER**
2629	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,417	CHO ET AL.	
	Examiner	Art Unit	
	GRANT D. SITTA	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-8 and 10-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/15/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/22/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Rilly et al (5,808,420) hereinafter Rilly.

3. In regards to claim 1, Rilly teaches a plasma display (abstract, "plasma display"), comprising: a panel (abstract, "screen or panel"); at least one voltage source (fig. 3 (V1 and V2)) for supplying a sustain voltage to the panel; an inductor (fig. 3 (L)) for recovering an energy stored in the panel by a resonance phenomenon such that the recovered energy is reusable for driving the panel; and first (fig. 3 (T4)) and second (fig. 3 (T4-)) switches arranged, in parallel (fig. 3 T14, T4-, and L parallel relationship), between the inductor and the panel (col. 3, lines 1-48)

wherein the inductor stores energy, recovered from the panel when the first switch is on (fig. 4 (T4)) and the inductor applies the stored energy to the panel when the second switch is on (fig. 4 (T4-)) (col. 4, lines 18-25).

4. In regards to claim 5, Rilly teaches an energy recovering (abstract, "recovery of the energy") method for a plasma display (abstract, "plasma display"), comprising:

forming a first electrically conductive path between a first voltage source (fig. V1 (col. 3, lines 1-48) and the plasma display using a first switch (fig. 3 one of switches T6s); forming a second electrically conductive path between a second voltage source (fig. 3 V2 (col. 3, lines 1-48).) and the plasma display using a second switch (fig. 3 one of switches T4)); forming a third electrically conductive path between the inductor and the plasma display using a third switch (fig. 3 (T1)); and forming a fourth electrically conductive path between the inductor and the plasma display using a fourth switch connected (fig. 3 T2), in parallel (fig. 3 T1, T2, and L parallel relationship), to the third switch (col. 3, lines 1-48).

5. In regards to claim 2, Rilly teaches wherein at least one voltage source comprises: a first voltage source for charging the panel to a first polarity voltage (fig. 3 (V1)); and a second voltage source (fig. 3 (V2)) for charging the panel to a second polarity voltage different from the first polarity voltage. ("It can be seen that the voltage values V2 and V1 are of different magnitude, for matching to the plasma screen, for example V2=120 volts and V1=-150 volts." Col. 3, lines 40-45).

6. In regards to claim 3, Rilly teaches further comprising: a third switch (fig. 3 (T1)) for forming a conductive path between the first voltage source (fig. 3 V1) and the panel; and a fourth switch (fig. 3 T2) for forming a conductive path between the second voltage source (fig. 3 V2) and the panel.

7. In regards to claim 4, Rilly teaches: a first diode connected between the first switch and the panel (fig. 3 D4); and a second diode connected between the second switch and the panel (fig. 3 D4 (-)).

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-8, 10-17, 19-31, 34,and 37-40 are rejected under 35 U.S.C. 102(e) as being anticapted by Lee et al (6,707,258) hereinafter, Lee.

10. In regards to claim 1, Lee teaches a plasma display, comprising:

a panel (fig. 1 (100)); at least one voltage source for supplying a sustain voltage to the panel (fig. 2 V1 and V2);

an inductor for recovering an energy stored in the panel by a resonance phenomenon (col. 4, lines 60-65) such that the recovered energy is reusable for driving the panel (fig. 2 L); and

first and second switches arranged, in parallel, between the inductor and the panels (fig. 2 S6 and S5)

wherein the inductor stores energy recovered from the panel when the first switch is on (fig. 3a S6 col. 5, lines 10-21) and the inductor applies the stored energy to the panel when the second switch is on (fig. 3a S5). Examiner points to fig. 4 Vx at panel capacitor Cp is increased M3 while S6 is on and decreases M5 when S5 is on. Col. 5, lines 1-67).

11. In regards to claim 5, Lee teaches an energy recovering method for a plasma display, comprising:

forming a first electrically conductive path between a first voltage source and the plasma display using a first switch (fig. 3B S6);

forming a second electrically conductive path between a second voltage source and the plasma display using a second switch (fig. 3E S5);

forming a third electrically conductive path between the inductor and the plasma display using a third switch (fig. 3D S1); and

forming a fourth electrically conductive path between the inductor and the plasma display using a fourth switch connected, in parallel, to the third switch (fig. 3A S2).

12. In regards to claim 7, Lee teaches a plasma display comprising (fig. 1 (100)):

a display having a plurality of electrodes and having a corresponding display capacitance between first and second nodes (fig. 2 Vx and Vy);

an inductor coupled to the second node and a third node (fig. 2 L);

a first switch coupled between the first and third nodes (fig. 2 S6); and

a second switch coupled between the first and third nodes (fig. 2 S5), the first and second switches being formed in parallel (fig. 2 S5 and S6 and col. 4, lines 42-46), wherein a first current path is formed via the panel capacitance, the second node, the inductor, the third node, the first switch and the first node (fig. 3B current path), and a second current path is formed via the panel capacitance, the first node, the second switch, the third node, the inductor and the second node (fig. 3E current path), and

wherein the second current path passes energy from the panel capacitance for storage in the inductor when the second switch is on (fig. 3a S5), and the first current path applies the stored energy, from the inductor to the panel capacitance when the first switch is on (fig. 3a S6 col. 5, lines 10-21). Examiner points to fig. 4 Vx at panel capacitor Cp is increased M3 while S6 is on and decreases M5 when S5 is on. Col. 5, lines 1-67).

13. In regards to claim 19, Lee teaches in display panels having panel electrodes and corresponding panel capacitance between first and second nodes, an inductor coupled to the second node and a third node, a first switch (fig. 2 (S6)) coupled between the first and third nodes and a second switch (fig. 2 (S5)) coupled between the first and third nodes, the first and second switches being formed in parallel (fig. 2 switches are in

parallel), an energy efficient method of driving said display panels through the inductor coupled to the panel electrodes (fig. 3A-F and col. 5, lines 1-67), comprising:

(a) discharging the panel capacitance through said inductor initially while storing energy in said inductor (abstract) until the magnitude of the inductor current reaches a maximum through a first current path formed via the panel capacitance (fig. 4 Vx and Vy), the second node, the inductor (fig. 2 L), the third node, the first switch and the first node, and secondly charging the panel capacitance through said inductor while removing the stored energy from said inductor until the inductor current reaches zero or before zero via the first current path (fig. 3B and 3E and col. 5 Modes 1-5 and fig. 4); and

(b) discharging the panel capacitance through said inductor initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum through a second current path formed via the panel capacitance, the fin:st node, the second switch, the third node, the inductor and the second node, and secondly charging the panel capacitance through said inductor while removing the stored energy from said inductor until the inductor current reaches zero or before zero through the second current paths (fig. 3B and 3E and col. 5 Modes 1-5 and fig. 4).

wherein said inductor stores said energy while the panel capacitance is clamped at first predetermined voltage and wherein said energy is removed from said inductor to cause the panel capacitance to change to a second predetermined voltage (fig. 4 Vx and Vy and IL).

14. In regards to claim 25, Lee teaches a plasma display panel driver circuit comprising:

a panel inter-electrode capacitor provided between at least one of a plurality of scanning electrodes and a plurality of sustain electrodes of a panel (col. 4, lines 12-21);

a charging/discharging circuit connected in series with said panel inter-electrode capacitor and between first and second nodes (col. 4, lines 12-21),

a clamping circuit having first and second switches for clamping a terminal voltage across the panel inter-electrode (fig. 2 S5and S6) capacitor to a first power source voltage level and to a second power source voltage level (fig. 2 V1 and V2), said first switch being connected in series between the first node and the first power source voltage level (fig. 2 S6 and V1), said second switch being connected in series between said first node and the second power source voltage level (fig. 2 S5 and V2), said inter-electrode capacitor being connected in series to the first and second nodes and said charging/discharging circuit and said clamping circuit being coupled in parallel between the first and second nodes (fig. 2 Cp) ,

wherein said charging/discharging circuit comprises a pair of switches coupled in parallel to each other between the first anode and a third node and an inductive coil coupled in series between the second and third nodes (fig. 2 L S5 and S6), and

wherein the inductive coil stores energy, recovered from the panel inter-electrode capacitor when a first one of the pair of switches is turned on and the inductive coil applies the stored energy to the panel inter-electrode capacitor when a

second one of the pair of switches is turned on (abstract and fig. 4 Vx and Vy).

15. In regards to claim 2, Lee teaches wherein at least one voltage source comprises:

a first voltage source for charging the panel to a first polarity (fig. 2 (V1)); and a second voltage source for charging the panel to a second polarity different from the first polarity voltage (fig. 2 V2).

16. In regards to claim 3, Lee teaches further comprising:
a third switch for forming a conductive path between the first voltage source and the panel (fig. 3A-F (S1)); and

a fourth switch for forming a conductive path between the second voltage source and the panel (fig. 3A-F (S2)).

17. In regards to claim 4, Lee teaches comprising: a first diode (fig. 3A-F D1) connected between the first switch and the panel (fig. 2 S6 and Cp); and

a second diode (fig. 3A–F D2) connected between the second switch and the panel (fig. 2 S5 and Cp).

18. In regards to claim 6, Lee teaches the energy recovering method, further shutting off a backward current from the plasma display using a first diode (fig. 2 (D1)) connected between the third switch and the plasma display (fig. 2 (S1 and Cp)); and

shutting off a backward current from the fourth switch using a second diode connected between the fourth switch and the plasma display (fig. 2 (D2)) and S2 col. 5, lines 1-67).

19. In regards to claim 8, Lee teaches wherein the direction of the first and second current paths are opposite directions (fig 3B and 3E the current flows in opposite directions).

20. In regards to claim 10, Lee teaches wherein the display capacitance is charged or discharged based on an LC resonance frequency (col. 5, lines 40-55).

21. In regards to claim 11, Lee teaches wherein the display capacitance is charged or discharged based on a non-LC resonance frequency (col. 4, lines 57-65). Examiner notes that variations of the mode are created by manipulation of the switches.

22. In regards to claim 12, Lee teaches wherein an energy of the inductor current is increased prior to the discharging of the display capacitance or the energy is decreased prior to charging of the display capacitance (fig. 4 Vx and Vy and IL).

23. In regards to claim 13, Lee teaches wherein during charging or discharging, the display capacitance is clamped before a stored energy of inductor reaches zero (fig. 4

Vx and Vy are clamped and thus the flat surface and IL).

24. In regards to claim 14, Lee teaches wherein the first current path further comprises a diode coupled between the first switch and the first node (fig. 3B D1).

25. In regards to claim 15, Lee teaches wherein the second current path further comprises a diode coupled between the first node and the second switch (fig. 3E D2).

26. In regards to claim 16, Lee teaches a plasma display further comprising: a first clamping circuit coupled between the first and second nodes (fig. 2 S1); and

a second clamping circuit coupled between the first and second nodes (fig. 2 S2).

27. In regards to claim 17, Lee teaches the plasma display of claim 16, wherein the first clamping circuit comprises a third switch coupled to the first node and a first potential via a first conductive path (fig. 4 S1), and the second clamping circuit comprises a fourth switch coupled to the first node and a second potential via a second conductive path (fig. 3 S2), wherein the first and second potentials are different (fig. 4 Vx and Vy V1 and V2).

28. In regards to claim 20, Lee teaches further comprising:

maintaining panel capacitance after step (a) by a first clamping circuit having a third switch coupled to the first node and a first potential via a first conductive path (fig. 4 S1); and

maintaining the panel capacitance after step (b) by a second clamping circuit having a fourth switch coupled to the first node and a second potential via a second conductive path (fig. 3 S2) and (fig. 4 Vx and Vy V1 and V2).

29. In regards to claim 21, Lee teaches wherein storing and removing of stored energy in the inductor is based on an LC resonance frequency if the inductor current reaches zero (col. 5, lines 40-55).

30. In regards to claim 22, Lee teaches wherein charging and discharging of the panel capacitance is not based on an LC resonance frequency via the first and second clamping circuit clamping the panel capacitance prior to the inductor current reaching zero (col. 4, lines 57-65). Examiner notes that variations of the mode are created by manipulation of the switches.

31. In regards to claim 23, Lee teaches wherein the first and second clamping circuits clamp the panel capacitance prior to the inductor current reaches zero (fig. 4 Vx and Vy clamp before IL reaches zero).

32. In regards to claim 24 Lee teaches wherein the second clamping circuit pre-stores energy in the inductor prior to step (a) and the first clamping circuit pre-stores energy in the inductor prior to step (b) (col. 5, lines 1-67 Mode 2 and Mode 5).

33. In regards to claim 26, Lee teaches wherein each of the pair of switches comprises a first transistor and a diode, and the pair of switches provide opposite current paths (fig. 3A-F D1 and D2).

34. In regards to claim 27, Lee teaches wherein the inter- electrode capacitor is charged/discharged based on an LC resonant frequency of the inductor coil and the inter-electrode capacitor (col. 4, lines 57-67).

35. In regards to claim 28, Lee teaches wherein the inter- electrode capacitor is charge/discharged based on a non-LC resonant frequency of the inductor coil and the inter-electrode capacitor (col. 4, lines 57-65). Examiner notes that variations of the mode are created by manipulation of the switches.

36. In regards to claim 29, Lee teaches wherein the clamping circuit clamps the inter-electrode capacitor one of the first and second power source voltage level prior to an energy of the inductor coil reaching zero (fig. 4 IL Vy).

37. In regards to claim 30, Lee teaches wherein the clamping circuit increases an energy of the inductor coil prior to charging/discharging of the inter-electrode capacitor (fig. 4 Vy and IL). Examiner notes that in step M5 IL is increased prior to the discharge of Vy) .

38. In regards to claim 31, Lee teaches wherein each of said first and second switches comprises a transistor (col. 4, lines 45-50 MOSFETs).

39. In regards to clam 34, Lee teaches wherein the panel includes a panel capacitor and wherein the inductor is the only circuit element for storing energy recovered from the panel capacitor (fig. 3A Cp and L).

40. In regard to claim 37, Lee teaches wherein the first switch has a first terminal coupled to the inductor and a second terminal coupled to the panel, and wherein the second switch has one terminal coupled to the first terminal of the first switch and another terminal coupled to the second terminal of the first switch (fig. 2 L, Cp, S5, and S6).

41. In regards to claim 38, Lee teaches, wherein the second terminal of the first switch is coupled to the panel through a first diode, and wherein said another terminal of the second switch is coupled to the panel through a second diode (fig. 2 S5, S6,D1 and

Cp).

42. In regards to claim 39, Lee teaches wherein the third switch has a first terminal coupled to the inductor and a second terminal coupled to the plasma display (fig. 2 S1 L and Cp), and wherein the fourth switch has one terminal coupled to the first terminal of the third switch and another terminal coupled to the second terminal of the third switch (fig. 2 S2 connected to S1 and Cp).

43. In regards to claim 40, Lee teaches wherein the second terminal of the third switch is coupled to the plasma display through a first diode, and wherein said another terminal of the fourth switch is coupled to the panel through a second diode (fig. 2 S2 D1, D2 and Cp).

Claim Rejections - 35 USC § 103

44. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

45. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

46. Claims 18, 32, 33, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Rilly et al (5,808,420) hereinafter, Rilly.

47. In regards to claim 18, Lee differs from the claimed invention in that Lee does not explicitly disclose wherein the first potential is provided by a positive power source, and the second potential is provided by a negative power source.

However, Rilly teaches a system and method for wherein the first potential is provided by a positive power source, and the second potential is provided by a negative power source. (fig. 4 V2 and V1 abstract, col. 3, lines 1-45 of Rilly).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Lee to include the use of a first potential provided by a positive power source, and the second potential is provided by a negative power source as taught by Rilly in order to provide a means of using both polarities in order to neutralize the information in the respective plasma pixels by a transition in the form of a sinusoidal half-cycle as stated in (col. 1, lines 28-46 of Rilly).

48. In regards to claim 32, Lee teaches wherein the first switch is turned on to allow the inductor to store energy recovered from the panel, the inductor storing the energy

during a time when the sustain voltage supplied to the panel is clamped (fig. 4 L ,S1, S2).

Lee differs from the claimed invention in that Lee does not explicitly disclose wherein a negative voltage is used.

However, Rilly teaches a system and method for wherein the first potential is provided by a positive power source, and the second potential is provided by a negative power source. (fig. 4 V2 and V1 abstract, col. 3, lines 1-45 of Rilly).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Lee to include the use of a first potential provided by a positive power source, and the second potential is provided by a negative power source as taught by Rilly in order to provide a means of using both polarities in order to neutralize the information in the respective plasma pixels by a transition in the form of a sinusoidal half-cycle as stated in (col. 1, lines 28-46 of Rilly).

49. In regards to claim 33, Lee as modified by Rilly teaches wherein the second switch is turned on to allow the inductor to apply the stored energy to the panel when the sustain voltage is to rise to a positive voltage (fig. 4 S6 and Vx Lee).

50. Claim 35 is rejected for the reasons of claims 32 and 33.

51. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee, in view of Lee et. al (US PUB 7,023,139) hereinafter, 139.

52. In regards to claim 36, Lee differs from the claimed invention in that Lee does not disclose wherein the first polarity voltage and the second polarity voltage have a same absolute value.

However, 139 teaches a system and method for wherein the first polarity voltage and the second polarity voltage have a same absolute value (fig. 2 Vs/2 and -Vs/2).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Lee to include the use of wherein the first polarity voltage and the second polarity voltage having a same absolute value as taught by 139 in order to prevent the voltage at each end of the inductor from being greater than the power supply and so that the rising time of the panel voltage is equal to the falling time as stated in (col. 2, lines 1-15 of 139).

Response to Arguments

53. Applicant's arguments filed 4/22/2008 in regards to claim 5 have been fully considered but they are not persuasive. On page 16, Applicant contends switches T1 and T2 of Rilly are coupled between inductor L and voltage source V2 and V1, not between inductor L and panel capacitor Cp (page 16, third and fourth full paragraph). Examiner respectfully disagrees. Claim 5 merely recites “forming a third electrically conductive path between the inductor and the plasma display using a third switch.” And

"forming a fourth electrically conductive path between the inductor and the plasma display using a fourth switch."Examiner contends that when T1 or T2 are closed a conductive path is formed between the inductor and the plasma display and V2 or V1. Claim 5 as currently written does not require the third switch or fourth switch to be directly connected between the inductor and Cp. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

54. Applicant's arguments with respect to claims 1-4, 6, 8, and 10-40 have been considered but are moot in view of the new ground(s) of rejection.

55. Examiner has changed his position in regards to the second switch, which was previously T2, now T4- which was necessitated by the amendment. However, in response to Applicant's remarks that Rilly does not disclose wherein the inductor stores energy recovered from the panel when the first switch is on (page 15, third paragraph), Examiner respectfully disagrees. As stated in col. 4, lines 15-25 of Rilly, Rilly teaches wherein the current I2 is switched on before the current is 1L is switched off, a current flows through the inductor L, and the current 1L stores energy in the inductance. I2 is switched on by the switches T4 and T6 in fig. 3.

Conclusion

56. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GRANT D. SITTA whose telephone number is (571)270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/GDS/
September 1, 2008